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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/966,440	09/27/2001	Akira Yamaguchi	2102475-991160	5355

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EXAMINER
MANDALA, VICTOR A

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 06/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/966,440	YAMAGUCHI ET AL.	
	Examiner	Art Unit	
	Victor A Mandala Jr.	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on *30 May 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *18-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☑ Claim(s) *18-21,24-32 and 35* is/are rejected.

7)☒ Claim(s) *22,23,33 and 34* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. The Applicant argues in Paper No. 8 that the 35 U.S.C 102 (b) rejection is invalid because it does not teach a first wiring layer but a metal filled via. The examiner has considered the applicant arguments but finds them to be non-persuasive because the first wiring layer as labeled, examiner's label #1 for simplicity to the Applicant, Duesman et al.'s label #142 in Paper No. 6 is seen as a wiring layer that connects the other wiring layers, examiner's label #2 for simplicity to the Applicant, Duesman et al.'s label #132. The examiner views the wiring layers #142 to extend in a vertical direct between the horizontal extending wiring layers #132. The examiner also views the wiring layer #132 as a layer that is larger in the vertical direction when compared to its horizontal. The Applicant's claimed language does not teach the direction the wiring layers extend and/or the minimum or maximum size limitations of the layers thus making the term layer as used in the applicant's claims broad. The claims 18-20, 24-28, 30-32, & 35 will be further rejected in a 35 U.S.C 103 (a) rejection below.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 18-20, 24-28, 30-32, & 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,078,100 Duesman et al.

2. Referring to claim 18, a semiconductor device comprising: a semiconductor substrate, (Figure 4a examiner's label #10); a first wiring layer, (Figure 4a examiner's label #1), having a first thickness and provided above the semiconductor substrate, (Figure 4a examiner's label #10); and a second wiring layer, (Figure 4a examiner's label #2), having a second thickness thinner than the first thickness and provided above the first wiring layer, (Figure 4a examiner's label #1).

3. Referring to claim 19, a semiconductor device, further comprising: a lowermost wiring layer, (Figure 4a examiner's label #4), nearest to the semiconductor substrate, (Figure 4a examiner's label #10), and provided below the first wiring layer, (Figure 4a examiner's label #1); and an uppermost layer, (Figure 4a #122), farthest from the semiconductor substrate, (Figure 4a examiner's label #10), and provided above the second wiring layer, (Figure 4a examiner's label #2).

4. Referring to claim 20, a semiconductor device, wherein a wiring pitch of the first wiring layer, (Figure 4a examiner's label #1), is greater than that of the second wiring layer, (Figure 4a examiner's label #2).

5. Referring to claim 24, a semiconductor device, wherein the first wiring layer, (Figure 4a examiner's label #1), is substantially as thick as the uppermost wiring layer, (Figure 4a #122).

6. Referring to claim 25, a semiconductor device, wherein the second wiring layer, (Figure 4a examiner's label #2), is substantially as thick as the lowermost wiring layer, (Figure 4a examiner's label #4).

7. Referring to claim 26, a semiconductor device, wherein all of the uppermost wiring layer, the lowermost wiring layer and the first and second wiring layers are metal layers. (Col. 2 Lines 9-11 & 13-14).

8. Referring to claim 27, a semiconductor device comprising; a semiconductor substrate, (Figure 4a examiner's label #10); an IP core area, (Figure 9), on the semiconductor substrate, (Figure 4a examiner's label #10); a peripheral area on the semiconductor substrate, (Figure 4a examiner's label #10), except for the IP core area, (Figure 9); a first wiring layer, (Figure 4a examiner's label #1), having a first thickness and provided above the semiconductor substrate, (Figure 4a examiner's label #10), in the IP core area, (Figure 9); and a second wiring layer, (Figure 4a examiner's label #2), having a second thickness smaller than the: first thickness and provided above the first wiring layer, (Figure 4a examiner's label #1), in the IP core area, (Figure 9).

9. Referring to claim 28, a semiconductor device, further comprising: a lowermost layer, (Figure 4a examiner's label #4), nearest to the semiconductor substrate, (Figure 4a examiner's label #10), and provided below the first wiring layer, (Figure 4a examiner's label #1); and an uppermost wiring layer, (Figure 4a #122), farthest from the semiconductor substrate, (Figure 4a examiner's label #10), and provided above the second wiring layer, (Figure 4a examiner's label #2).

10. Referring to claim 30, a semiconductor device, wherein a wiring pitch of the first wiring layer, (Figure 4a examiner's label #1), is greater than that of the second wiring layer, (Figure 4a examiner's label #2).

11. Referring to claim 31, a semiconductor device, wherein the first wiring layer, (Figure 4a examiner's label #1), is substantially as thick as the uppermost wiring layer, (Figure 4a #122).

12. Referring to claim 32, a semiconductor device, wherein the second wiring layer, (Figure 4a examiner's label #2), is substantially as thick as the lowermost wiring layer, (Figure 4a examiner's label #4).

13. Referring to claim 35, a semiconductor device, wherein all of the uppermost wiring layer, (Figure 4a #122), the lowermost wiring layer, (Figure 4a examiner's label #4), and the first and second wiring layers, (Figure 4a examiner's label #1 & 2), are metal layers, (Col. 2 Lines 9-11 & 13-14).

14. The indicated allowability of claims 21 and 29 are withdrawn in view of the newly discovered reference(s) to U.S. Patent No. 5,488,542 Ito. Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 18-21, 26-30, & 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,488,542 Ito.

15. Referring to claim 18, a semiconductor device comprising: a semiconductor substrate, (Figure 6 #10 and see ** below); a first wiring layer, (Figure 3 & 6 #13), having a first thickness and provided above the semiconductor substrate, (Figure 6 #10 and see ** below); and a second wiring layer, (Figure 6 examiner's label #31b), having a second thickness thinner than the first thickness and provided above the first wiring layer, (Figure 3 & 6 #13).

** Ito discloses the claimed invention except for substrate being made out of a semiconductor material. It would have been obvious to one having ordinary skill in the art at the time the invention was made to make the substrate out of a semiconductor material instead of a the disclosed ceramic material, (Col. 3 Line 3 and Col. 1 Lines 46-51), since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

16. Referring to claim 19, a semiconductor device, further comprising: a lowermost wiring layer, (Figure 3 & 6 #12), nearest to the semiconductor substrate, (Figure 6 #10 and see ** above), and provided below the first wiring layer, (Figure 3 & 6 #13); and an uppermost layer, (Figure 6 examiner's label #31a), farthest from the semiconductor substrate, (Figure 6 #10 and see ** above), and provided above the second wiring layer, (Figure 6 examiner's label #31b).

17. Referring to claim 20, a semiconductor device, wherein a wiring pitch, (Figure 6 examiner's label #P2), of the first wiring layer, (Figure 3 & 6 #13), is greater than that, (Figure 6 examiner's label #P1), of the second wiring layer, (Figure 6 examiner's label #31b).

18. Referring to claim 21, a semiconductor device, wherein the first wiring layer, (Figure 3 & 6 #13), is a layer on which a power source line, (Col. 4 Line 57), is formed.

19. Referring to claim 26, a semiconductor device, wherein all of the uppermost wiring layer, the lowermost wiring layer and the first and second wiring layers are metal layers, (Col. 5 Lines 21-22).

20. Referring to claim 27, a semiconductor device comprising; a semiconductor substrate, (Figure 6 #10 and see ** below); an IP core area, (Figure 6 #40), on the semiconductor substrate, (Figure 6 #10 and see ** below); a peripheral area on the semiconductor substrate, (Figure 6 #10 and see ** below), except for the IP core area, (Figure 6 #40); a first wiring layer, (Figure 3 & 6 #13), having a first thickness and provided above the semiconductor substrate, (Figure 6 #10 and see ** below), in the IP core area, (Figure 6 #40); and a second wiring layer, (Figure 6 examiner's label #31b), having a second thickness smaller than the: first thickness and provided above the first wiring layer, (Figure 3 & 6 #13), in the IP core area, (Figure 6 #40).

** Ito discloses the claimed invention except for substrate being made out of a semiconductor material. It would have been obvious to one having ordinary skill in the art at the time the invention was made to make the substrate out of a semiconductor material instead of a the disclosed ceramic material, (Col. 3 Line 3 and Col. 1 Lines 46-51), since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

21. Referring to claim 28, a semiconductor device, further comprising: a lowermost layer, (Figure 3 & 6 #12), nearest to the semiconductor substrate, (Figure 6 #10 and see ** above), and provided below the first wiring layer, (Figure 3 & 6 #13); and an uppermost wiring layer, (Figure 6 examiner's label #31a), farthest from the semiconductor substrate, (Figure 6 #10 and see ** above), and provided above the second wiring layer, (Figure 6 examiner's label #31b).

21. Referring to claim 29, a semiconductor device, wherein the first wiring layer, (Figure 3 & 6 #13), is a layer on which a core power source line formed, (Col. 4 line 57).

22. Referring to claim 30, a semiconductor device, wherein a wiring pitch, (Figure 6 examiner's label #P2), of the first wiring layer, (Figure 3 & 6 #13), is greater than that, (Figure 6 examiner's label #P1), of the second wiring layer, (Figure 6 examiner's label #31b).

23. Referring to claim 35, a semiconductor device, wherein all of the uppermost wiring layer the lowermost wiring layer and the first and second wiring layers are metal layers, (Col. 5 Lines 21-22).

Allowable Subject Matter

24. Claims 22-23 & 33-34 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor A Mandala Jr. whose telephone number is (703) 308-6560. The examiner can normally be reached on Monday through Thursday from 8am till 6pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

VAMJ
June 13, 2003